

What is claimed is:

1. An offset voltage correction apparatus comprising:

a comparator circuit with a first internal node having a potential varied in response to a potential at a first input terminal and with a second internal node having a potential varied in response to a potential at a second input terminal, said comparator circuit comparing the potential at said first internal node with the potential at said second internal node to output a comparison result as a comparison result signal;

an offset voltage detection signal output part sequentially converting a counter value obtained through an up-count operation and a down-count operation on a clock signal to an offset voltage detection signal to provide the offset voltage detection signal to said second input terminal of said comparator circuit having a reference signal directed to said first input terminal;

an offset voltage correction signal generator performing a predetermined arithmetic operation, in which a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output part and a counter value provided when a

change has occurred in logic level of said comparison result signal during the down-count operation on the clock signal by said offset voltage detection signal output part are used, generating an offset voltage correction signal in accordance with an arithmetic operation result counter value obtained by the arithmetic operation; and

an offset voltage adjuster adjusting any one of the potential at said first internal node and the potential at said second internal node in accordance with said offset voltage correction signal.

2. The offset voltage correction apparatus according to claim 1, wherein

said offset voltage adjuster comprises a control terminal receiving said offset voltage correction signal, a first power supply terminal connected to a power supply node, and a transistor having a second power supply terminal connected to any one of said first internal node and said second internal node.

3. The offset voltage correction apparatus according to claim 1, wherein

said offset voltage adjuster is contained in a first internal node potential control device, to control the potential at said first internal node in response to the potential at said first input terminal, and

said first internal node potential control

device comprises:

a first control terminal connected to said first input terminal;

a second control terminal receiving said offset voltage correction signal;

a first power supply terminal connected to a power supply node; and

a transistor having a second power supply terminal connected to said first internal node.

4. The offset voltage correction apparatus according to claim 1, wherein

said offset voltage adjuster is contained in a second internal node potential control device, to control the potential at said second internal node in response to the potential at said second input terminal, and

said second internal node potential control device comprises:

a first control terminal connected to said second input terminal;

a second control terminal receiving said offset voltage correction signal;

a first power supply terminal connected to a power supply node; and

a transistor having a second power supply terminal connected to said second internal node.

5. The offset voltage correction apparatus according

to claim 1, wherein

    said arithmetic operation result counter value is an average value of a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output part and a counter value provided when a change has occurred in logic level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output part.

6. The offset voltage correction apparatus according to claim 2, wherein

    said arithmetic operation result counter value is an average value of a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output part and a counter value provided when a change has occurred in logic level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output part.

7. The offset voltage correction apparatus according to claim 3, wherein

    said arithmetic operation result counter value is an average value of a counter value provided when

a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output part and a counter value provided when a change has occurred in logic level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output part.

8. The offset voltage correction apparatus according to claim 4, wherein

said arithmetic operation result counter value is an average value of a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output part and a counter value provided when a change has occurred in logic level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output part.

9. An offset voltage correction apparatus comprising:

a comparator circuit with a first internal node having a potential varied in response to a potential at a first input terminal and with a second internal node having a potential varied in response to a potential at a second input terminal, said

comparator circuit comparing the potential at said first internal node with the potential at said second internal node to output a comparison result as a comparison result signal;

offset voltage detection signal output means for sequentially converting a counter value obtained through an up-count operation and a down-count operation on a clock signal to an offset voltage detection signal to provide the offset voltage detection signal to said second input terminal of said comparator circuit having a reference signal directed to said first input terminal;

offset voltage correction signal generation means for performing a predetermined arithmetic operation, using a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output means and using a counter value provided when a change has occurred in logic level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output means, to generate an offset voltage correction signal in accordance with an arithmetic operation result counter value obtained by the arithmetic operation; and

offset voltage adjustment means for adjusting any one of the potential at said first internal node and the potential at said second internal node in accordance with said offset voltage correction signal.

10. The offset voltage correction apparatus according to claim 9, wherein

said offset voltage adjustment means comprises a control terminal for receiving said offset voltage correction signal, a first power supply terminal connected to a power supply node, and a transistor having a second power supply terminal connected to any one of said first internal node and said second internal node.

11. The offset voltage correction apparatus according to claim 9, wherein

said offset voltage adjustment means is contained in first internal node potential control means for controlling the potential at said first internal node in response to the potential at said first input terminal, and

said first internal node potential control means comprises:

a first control terminal connected to said first input terminal;

a second control terminal for receiving said offset voltage correction signal;

a first power supply terminal connected to a power supply node; and

a transistor having a second power supply terminal connected to said first internal node.

12. The offset voltage correction apparatus according to claim 9, wherein

said offset voltage adjustment means is contained in second internal node potential control means for controlling the potential at said second internal node in response to the potential at said second input terminal, and

said second internal node potential control means comprises:

a first control terminal connected to said second input terminal;

a second control terminal for receiving said offset voltage correction signal;

a first power supply terminal connected to a power supply node; and

a transistor having a second power supply terminal connected to said second internal node.

13. The offset voltage correction apparatus according to claim 9, wherein

said arithmetic operation result counter value is an average value of a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count

operation on said clock signal by said offset voltage detection signal output means and a counter value provided when a change has occurred in logic level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output means.

14. The offset voltage correction apparatus according to claim 10, wherein

    said arithmetic operation result counter value is an average value of a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output means and a counter value provided when a change has occurred in logic level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output means.

15. The offset voltage correction apparatus according to claim 11, wherein

    said arithmetic operation result counter value is an average value of a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output means and a counter value provided when a change has occurred in logic

level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output means.

16. The offset voltage correction apparatus according to claim 12, wherein

    said arithmetic operation result counter value is an average value of a counter value provided when a change has occurred in logic level of said comparison result signal during the up-count operation on said clock signal by said offset voltage detection signal output means and a counter value provided when a change has occurred in logic level of said comparison result signal during the down-count operation on said clock signal by said offset voltage detection signal output means.